CLAIMS

1. A method of forming an array of memory cells comprising:

forming a series of capacitor constructions, the capacitor constructions having storage nodes; the capacitor constructions being defined to include a first set of capacitor constructions and a second set of capacitor constructions;

forming a series of electrically conductive transistor gates over the capacitor constructions and in electrical connection with the capacitor constructions; the transistor gates being defined to include a first set that is in electrical connection with the storage nodes of the first set of capacitor constructions, and a second set that is in electrical connection with the storage nodes of the second set of capacitor constructions;

forming a first conductive line over the transistor gates and in electrical connection with the first set of transistor gates; and

forming a second conductive line over the first conductive line and in electrical connection with the second set of transistor gates.

2. The method of claim 1 further comprising, before forming the series of electrically conductive transistor gates, forming a layer of silicon dioxide over the capacitor constructions; and wherein the electrically conductive transistor gates are formed over the layer of silicon dioxide.

3. The method of claim 1 further comprising:

forming openings extending through the first conductive line and to the second set of conductive transistor gates;

forming sidewall spacers within the openings to cover exposed sidewalls of the first conductive line; and

forming conductive material within the openings, the conductive material electrically connecting the second conductive lines to the second set of conductive transistor gates.

4. The method of claim 3 wherein the conductive material is formed within the openings during formation of the second conductive lines.

5. The method of claim 3 wherein the conductive material comprises conductively-doped silicon.

6. The method of claim 1 wherein the first and second conductive lines comprise conductively-doped silicon.

7. The method of claim 1 further comprising, prior to forming the first conductive line:

forming a layer of insulative material over the conductive transistor gates; and

removing the insulative material from over at least portions of the first transistor gates while not removing the insulative material from over the second transistor gates.

8. The method of claim 7 wherein the insulative material comprises silicon nitride.

9. The method of claim 1 further comprising forming a layer of insulative material over the first conductive lines prior to forming the second conductive lines; the second conductive lines being electrically isolated from the first conductive lines by at least the insulative material.

10. The method of claim 9 wherein the insulative material comprises silicon nitride.

11. The method of claim 1 further comprising forming bitline interconnections proximate at least some of the transistor gates and electrically connected through the transistor gates to the capacitor constructions.

12. The method of claim 1 wherein a semiconductive material is over the capacitor constructions, and wherein the transistor gates are over the semiconductive material, the method further comprising:

forming conductively doped source/drain regions within the semiconductive material, the source/drain regions being formed proximate at least some of the transistor gates;

forming protective blocks over the source/drain regions prior to forming the second conductive line;

after forming the second conductive line, removing at least a portion of at least some of the protective blocks to form openings extending substantially to at least some of the source/drain regions;

forming bitline interconnections within the openings and electrically connected through the transistor gates to the capacitor constructions.

13. The method of claim 12 wherein the protective blocks comprise silicon dioxide.

14. A method of forming an array of memory cells comprising:

forming a series of capacitor constructions, the capacitor constructions having storage nodes; the capacitor constructions being defined to include a first set and a second set;

forming an electrically conductive material over the capacitor constructions and in electrical connection with the storage nodes of the capacitor constructions;

forming a first conductive line over the conductive material and in electrical connection with the first set of capacitor constructions through the conductive material; and

forming a second conductive line over the first conductive line and in electrical connection with the second set of capacitor constructions through the conductive material; the second conductive line being electrically connected with the conductive material through conductive interconnects extending within openings in the first conductive line.

15. The method of claim 14 further comprising, before forming the conductive transistor material, forming a layer of silicon dioxide over the capacitor constructions; and wherein the conductive material is formed over the layer of silicon dioxide.

16. The method of claim 14 wherein the openings in the first conductive line are formed prior to formation of the second conductive line, wherein the openings comprise peripheries which include exposed portions of the first conductive line, the method further comprising:

forming sidewall spacers within the openings to cover the exposed portions of the first conductive line; and

forming conductive interconnects within the openings, the conductive interconnects electrically connecting the second conductive lines to the conductive material.

17. The method of claim 16 wherein the conductive interconnects are formed within the openings during formation of the second conductive lines.

18. The method of claim 16 wherein the conductive interconnects comprise conductively-doped silicon.

19. The method of claim 14 wherein the first and second conductive lines comprise conductively-doped silicon.

20. The method of claim 14 further comprising, prior to forming the first conductive line:

forming a layer of insulative material over the conductive material;

removing the insulative material from over first portions of the conductive material to expose the first portions, while not removing the insulative material from over second portions of the conductive material;

wherein the first conductive line is formed over and physically against the exposed first portions of the conductive material; and

wherein the first conductive line is formed over the second portions of the conductive material, and is separated from the second portions of the conductive material by the insulative material.

21. The method of claim 20 wherein the insulative material comprises silicon nitride.

22. The method of claim 14 further comprising forming a layer of insulative material over the first conductive lines prior to forming the second conductive lines; the second conductive lines being electrically isolated from the first conductive lines by at least the insulative material.

23. The method of claim 22 wherein the insulative material comprises silicon nitride.

24. A method of forming an array of memory cells comprising:

forming a series of capacitor constructions supported by a monocrystalline silicon substrate, the capacitor constructions having storage nodes; the capacitor constructions being defined to include a first set of capacitor constructions and a second set of capacitor constructions; the substrate having a damage region therein;

after forming the capacitor constructions, breaking the substrate along the damage region;

after breaking the substrate, forming a series of transistor gates over the capacitor constructions and in electrical connection with the capacitor constructions; the transistor gates being defined to include a first set that is in electrical connection with the storage nodes of the first set of capacitor constructions, and a second set that is in electrical connection with the storage nodes of the second set of capacitor constructions;

forming a first conductive line over the transistor gates and in electrical connection with the first set of transistor gates; and

forming a second conductive line over the first conductive line and in electrical connection with the second set of transistor gates.

25. The method of claim 24 further comprising, before forming the series of electrically conductive transistor gates, forming a layer of silicon dioxide over the capacitor constructions; and wherein the electrically conductive transistor gates are formed over the layer of silicon dioxide.

26. The method of claim 24 further comprising:

forming openings extending through the first conductive line and to the second set of conductive transistor gates;

forming sidewall spacers within the openings to cover exposed sidewalls of the first conductive line; and

forming conductive material within the openings, the conductive material electrically connecting the second conductive lines to the second set of conductive transistor gates.

27. The method of claim 26 wherein the conductive material is formed within the openings during formation of the second conductive lines.

28. The method of claim 24 wherein the first and second conductive lines comprise conductively-doped silicon.

29. The method of claim 24 further comprising, prior to forming the first conductive line:

forming a layer of insulative material over the conductive transistor gates; and

removing the insulative material from over at least portions of the first transistor gates while not removing the insulative material from over the second transistor gates.

30. The method of claim 29 wherein the insulative material comprises silicon nitride.

31. The method of claim 24 further comprising forming a layer of insulative material over the first conductive lines prior to forming the second conductive lines; the second conductive lines being electrically isolated from the first conductive lines by at least the insulative material.

32. The method of claim 31 wherein the insulative material comprises silicon nitride.

33. The method of claim 24 further comprising forming bitline interconnections proximate at least some of the transistor gates and electrically connected through the transistor gates to the capacitor constructions.

34. The method of claim 24 wherein a semiconductive material is over the capacitor constructions, and wherein the transistor gates are over the semiconductive material, the method further comprising:

forming conductively doped source/drain regions within the semiconductive material, the source/drain regions being formed proximate at least some of the transistor gates;

forming protective blocks over the source/drain regions prior to forming the second conductive line;

after forming the second conductive line, removing at least a portion of at least some of the protective blocks to form openings extending substantially to at least some of the source/drain regions; and

forming bitline interconnections within the openings and electrically connected through the transistor gates to the capacitor constructions.

35. The method of claim 34 wherein the protective blocks comprise silicon dioxide.

36. An array of memory cells comprising:

a series of capacitor constructions, the capacitor constructions having storage nodes; the capacitor constructions being defined to include a first set of capacitor constructions and a second set of capacitor constructions;

a series of transistor gates over the capacitor constructions and in electrical connection with the capacitor constructions; the transistor gates being defined to include a first set that is in electrical connection with the storage nodes of the first set of capacitor constructions, and a second set that is in electrical connection with the storage nodes of the second set of capacitor constructions;

a first conductive line over the transistor gates and in electrical connection with the first set of transistor gates, the first conductive line not being in electrical connection with the second set of transistor gates; and

a second conductive line over the first conductive line and in electrical connection with the second set of transistor gates, the second conductive line not being in electrical connection with the first set of transistor gates.

37. The array of claim 36 further comprising a layer of silicon dioxide between the capacitor constructions and the electrically conductive transistor gates.

38. The array of claim 36 further comprising:

openings extending through the first conductive line and to the second set of conductive transistor gates;

sidewall spacers within the openings and narrowing the openings; and

conductive material within the narrowed openings, the conductive material electrically connecting the second conductive lines to the second set of conductive transistor gates.

39. The array of claim 38 wherein the conductive material comprises conductively-doped silicon.

40. The array of claim 36 wherein the first and second conductive lines comprise conductively-doped silicon.

41. The array of claim 36 wherein the first conductive line is physically against the first conductive transistor gates, and further comprising a layer of insulative material over the second set of conductive transistor gates; the insulative material physically and electrically separating the second set of transistor gates from the first conductive line.

42. The array of claim 41 wherein the insulative material comprises silicon nitride.

43. The array of claim 36 further comprising bitline interconnections proximate at least some of the transistor gates and electrically connected through the transistor gates to the capacitor constructions.

44. The array of claim 36 wherein a semiconductive material is over the capacitor constructions, and wherein the transistor gates are over the semiconductive material, the array further comprising:

conductively doped source/drain regions within the semiconductive material, the source/drain regions being proximate at least some of the transistor gates;

openings extending through the first and second conductive lines and to the source/drain regions; and

bitline interconnections within the openings and electrically connected through the transistor gates to the capacitor constructions.

45. An array of memory cells comprising:

a series of capacitor constructions, the capacitor constructions having storage nodes; the capacitor constructions being defined to include a first set and a second set;

a conductive material over the capacitor constructions and in electrical connection with the storage nodes of the capacitor constructions;

a first conductive line over the conductive material and in electrical connection with the first set of capacitor constructions through the conductive material; and

a second conductive line over the first conductive line and in electrical connection with the second set of capacitor constructions through the conductive material; the second conductive line being electrically connected with the conductive material through conductive interconnects extending within openings in the first conductive line.

46. The array of claim 45 further comprising a layer of silicon dioxide between the capacitor constructions and the conductive material.

47. The array of claim 45 wherein electrically insulative sidewall spacers are within the openings and between the conductive interconnects and the first conductive line.

48. The array of claim 47 wherein the conductive interconnects comprise conductively-doped silicon.

49. The array of claim 45 wherein the first and second conductive lines comprise conductively-doped silicon.

50. The array of claim 45 further comprising a layer of insulative material between the first and second conductive lines; the second conductive lines being electrically isolated from the first conductive lines by at least the insulative material.

51. The array of claim 50 wherein the insulative material comprises silicon nitride.